IN THE CLAIMS:

Listing of claims:

1-19 (canceled)

20. (previously presented) A method as in claim 24, wherein the first layer comprises an epitaxial growth layer.

21. (previously presented) A method as in claim 24, further comprising removing the polishing stopper layer after planarizing the dielectric layer.

22. (previously presented) A method as in claim 24, further comprising oxidizing at least a portion of the first layer in the at least one trench prior to forming the dielectric layer in and above the trench.

23. (original) A method as in claim 22, further comprising forming a pad layer between the first layer and the polishing stopper layer.

24. (currently amended) A method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor substrate having a first layer thereon ;

forming a pad layer on the first layer;

forming a polishing stopper layer on the pad layer;

forming at least one trench by etching the first layer while using at least the polishing stopper layer as a mask;

forming a dielectric layer in and above the trench;

planarizing the dielectric layer using the polishing stopper layer as a stopper;

removing the polishing stopper layer after planarizing the dielectric layer;

removing the pad layer after the removing the polishing stopper layer;

forming a sacrificial oxide layer on the first layer after the removing the pad layer;

thermally treating the dielectric layer at a temperature of at least 1050°C after the forming the sacrificial oxide layer; and

after the thermally treating the dielectric layer at a temperature of at least 1050°C, implanting impurities to form a well in the first layer ~~adjacent to the trench~~.

25. (previously presented) A method as in claim 24, wherein the thermally treating the dielectric layer is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen.

26. (previously presented) A method as in claim 24, wherein the dielectric layer is formed using high density plasma chemical vapor deposition.

27-31. (canceled)

32. (previously presented) A method for manufacturing a semiconductor device, comprising:

providing a semiconductor layer;

forming a plurality of trenches in the semiconductor layer;

forming a thermal oxide layer on the semiconductor layer in the trenches;

depositing a dielectric layer into the trenches and filling the trenches with the dielectric layer;

thermally treating the dielectric layer in the trenches at a temperature of at least 1050°C; and

after the thermally treating the dielectric layer in the trenches, forming a well region between a first trench and a second trench of the plurality of trenches, wherein the first trench is adjacent to the second trench, and wherein the well region is formed to extend continuously in the semiconductor layer from the first trench to the second trench.

33. (previously presented) A method according to claim 32, wherein the dielectric layer is formed in direct contact with the thermal oxide layer in the trenches.

34. (previously presented) A method according to claim 33, wherein the dielectric layer is formed with a film density of at least $2.1 g/cm^3$.

35. (previously presented) A method according to claim 34, wherein the dielectric layer is formed by a high density plasma CVD method.

36. (previously presented) A method according to claim 35, wherein the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate.

37. (previously presented) A method according to claim 36, wherein the epitaxial growth layer has a thickness of at least 2 μm.

38. (previously presented) A method according to claim 32, further comprising:

forming a polishing stopper layer on the semiconductor layer prior to forming the plurality of trenches;

forming openings in the polishing stopper layer above the regions in the semiconductor layer where the plurality of trenches are to be formed;

forming the dielectric layer in the openings and on the polishing stopper layer,

planarizing the dielectric layer using the polishing stopper layer as a stop; and

removing the polishing stopper layer after planarizing the dielectric layer and prior to the thermally treating the dielectric layer.

39. (previously presented) A method according to claim 38, further comprising forming an oxide pad layer on the semiconductor layer prior to forming the polishing stopper layer.

40. (currently amended) A method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a polishing stopper layer on a semiconductor layer;

forming an opening in the polishing stopper layer and a trench in the semiconductor layer;

forming a dielectric layer in the trench, in the opening in the stopper layer, and on the stopper layer;

planarizing the dielectric layer using the polishing stopper layer as a stop;

removing the polishing stopper layer after the planarizing the dielectric layer;

conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer, wherein the thermal treatment is conducted at a temperature of at least 1050°C; and

~~forming a well in the semiconductor layer~~ implanting impurity ions into the semiconductor layer after the thermal treatment of the dielectric layer.

41. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, further comprising forming a pad layer on the semiconductor layer prior to forming the polishing stopper layer, wherein the pad layer is formed between and in direct contact with the semiconductor layer and the polishing stopper layer.

42. (previously presented) A method according to claim 41, wherein the opening in the polishing stopper layer also extends through the pad layer.

43. (previously presented) A method according to claim 42, further comprising isotropically etching the pad layer and upper portions of the dielectric layer after the removing the polishing stopper layer and prior to the conducting the thermal treatment.

44. (currently amended) A method ~~according to claim 43,~~ for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a polishing stopper layer on a semiconductor layer;

forming an opening in the polishing stopper layer and a trench in the semiconductor layer;

forming a pad layer on the semiconductor layer prior to forming the polishing stopper layer, wherein the pad layer is formed between and in direct contact with the semiconductor layer and the polishing stopper layer, and wherein the opening in the polishing stopper layer also extends through the pad layer;

forming a dielectric layer in the trench, in the opening in the stopper layer and the pad layer, and on the stopper layer;

planarizing the dielectric layer using the polishing stopper layer as a stop;

removing the polishing stopper layer after the planarizing the dielectric layer;

conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer, wherein the thermal treatment is conducted at a temperature of at least 1050°C;

forming a well in the semiconductor layer after the thermal treatment of the dielectric layer;

isotropically etching the pad layer and upper portions of the dielectric layer after the removing the polishing stopper layer and prior to the conducting the thermal treatment, wherein the isotropically etching exposes upper surfaces of the semiconductor layer.

45. (previously presented) A method according to claim 44, wherein an oxide layer is formed on the exposed upper surfaces of the semiconductor layer after the isotropically etching and prior to the forming a well in the semiconductor layer.

46. (previously presented) A method according to claim 45, wherein the oxide layer is formed prior to the conducting a thermal treatment of the dielectric layer.

47. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the dielectric layer is formed with a film density of at least $2.1 g/cm^3$.

48. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the temperature of the thermal treatment is 1100°C or higher.

49. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the temperature of the thermal treatment is in the range of 1050°C to 1250°C.

50. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the dielectric layer is formed by a high density plasma CVD method.

51. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer thereon, wherein the dielectric layer is formed in direct contact with the thermal oxide layer.

52. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 51, wherein the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700°C to 1150°C.

53. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 51, wherein the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of 950 to 1150°C.

54. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 51, wherein the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm.

55. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate.

56. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 40, wherein the trench is formed with a trench width of no greater than 0.35 μm.

57-59. (canceled)

60. (currently amended) A method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor layer;

forming a pad oxide layer on the semiconductor layer;

forming a polishing stopper layer in direct contact with the pad oxide layer, wherein the pad oxide layer is positioned between the semiconductor layer and the polishing stopper layer;

forming a patterned resist layer on the polishing stopper layer, the patterned resist layer including an open region exposing part of the polishing stopper layer over a trench formation region;

using the patterned resist layer as a mask, etching the polishing stopper layer and the pad oxide layer so that a portion of the semiconductor layer is exposed;

after the etching removing the patterned resist layer;

after the removing the patterned resist layer, etching the semiconductor layer to form at least one trench therein, using the polishing stopper layer as a mask;

forming a dielectric layer in and above the at least one trench;

planarizing the dielectric layer using the polishing stopper layer as a stopper;

removing the polishing stopper layer and the pad oxide layer; ~~and~~

heating the dielectric layer to a temperature of at least 1050°C; and

after the heating the dielectric layer to a temperature of at least 1050°C, implanting impurity ions into the semiconductor layer to form a well in the semiconductor substrate.

61. (previously presented) A method according to claim 60, further comprising, after forming the at least one trench and prior to forming the dielectric layer, forming a thermal oxide layer on the semiconductor substrate in the at least one trench.

62. (canceled)